In the Claims:

1. (Original) An integrated circuit device, comprising:

a CAM array block that is configured to perform a search operation in a staged segment-to-segment manner using a plurality of hybrid comparands that are pipelined into said CAM array block during consecutive stages of the search operation, with each of the plurality of hybrid comparands comprising a virtual sector field and a data field.

2. (Original) The device of Claim 1, wherein said CAM array block is responsive to a segment address, which identifies an active segment of CAM cells in said CAM array block.

3. (Original) The device of Claim 1, wherein said CAM array block comprises:

a CAM array; and

a global mask cell sub-array that is electrically coupled to said CAM array.

4. (Original) The device of Claim 3, wherein said CAM array block further comprises:

a bit/data line control circuit that is electrically coupled to said CAM array by bit lines and data lines and has inputs that are responsive mask assertion signals generated by said global mask cell sub-array.

5. (Original) The device of Claim 2, wherein the data field is derived from a first portion of an input address; and wherein the virtual sector field and the segment address are derived from a second portion of the input address.

6. (Original) An integrated circuit device, comprising:

a CAM array block that is configured to perform a search operation in a staged segment-to-segment manner using a plurality of comparands that are pipelined into said CAM array block during consecutive stages of the search operation, said CAM array block comprising at least one multi-segment CAM array and a global mask cell sub-array that is responsive to a segment address.

7. (Original) The device of Claim 6, wherein said global mask cell sub-array is responsive to a mode select signal.

8. (Original) The device of Claim 6, wherein the comparands are hybrid comparands that comprise a virtual sector field and a data field.

9. (Original) An integrated circuit system, comprising:

a programmable address translation unit that is configured to generate a CAM segment address and a virtual sector address in response to a first portion of an input address; and

a CAM device that is responsive to the CAM segment address and is configured to treat the virtual sector address and a second portion of the input address as respective fields of a search word during pipelined search operations.

10. (Original) The system of Claim 9, wherein said CAM device comprises a CAM array block having a global mask cell sub-array therein that is responsive to the CAM segment address.

11. (Original) A content address memory (CAM) device, comprising:

a CAM array having a plurality of segments therein;

a bit/data line control circuit that is electrically coupled to said CAM array by bit lines and data lines; and

a global mask cell sub-array that is electrically coupled to said bit/data line control circuit and is responsive to a segment address signal that designates which ones of the plurality of segments are active and which other ones of the plurality of segments are globally masked during a staged segment-to-segment search operation.

12. (Original) The CAM device of Claim 11, wherein said global mask cell sub-array is further responsive to a mode select signal that specifies an active width of search words applied to said CAM array during search operations.

13. (Original) The CAM device of Claim 11, wherein said global mask cell sub-array is electrically coupled to the bit lines.

14. (Original) An integrated circuit system, comprising:

a programmable address translation unit that is configured to generate a CAM segment address in response to a first portion of an input address; and

a CAM device that is responsive to a second portion of the input address, said CAM device comprising:

a segmented CAM array; and

a global mask cell sub-array that is configured to specify location of global masks provided to said segmented CAM array during search operations and is responsive to the CAM segment address.

15. (Original) The system of Claim 14, wherein the CAM segment address designates which portions of said segmented CAM array are actively searched and which other portions of said segmented CAM array are globally masked during a respective search operation.

16. (Original) The system of Claim 14, wherein said CAM device further comprises a bit/data line control circuit that is electrically coupled to said segmented CAM array by bit lines and data lines.

17. (Original) The system of Claim 16, wherein said bit/data line control circuit is configured to receive mask assertion signals from said global mask cell sub-array.

18. (Original) The system of Claim 14, wherein said global mask cell sub-array is responsive to a mode select signal.

19. (Original) The system of Claim 14, wherein said segmented CAM array comprises XY ternary CAM cells.

20. (Original) The system of Claim 14, wherein said global mask cell sub-array comprises hard and soft mask cells therein.

21. (Original) The system of Claim 14, wherein said programmable address translation unit is further configured to generate a virtual sector address in response to the first portion of the input address; and wherein said CAM device is configured to treat the second portion of the input address and the virtual sector address as a hybrid comparand during a search operation.

22. (Original) A method of operating a CAM array, comprising the step of:

performing a search operation in a staged segment-to-segment manner across a CAM array using a plurality of hybrid comparands that are pipelined into the CAM array during consecutive stages of the search operation, with each of the plurality of hybrid comparands comprising a virtual sector field and a data field.

23. (Original) The method of Claim 22, wherein said performing step comprises:

applying a virtual sector field of a first hybrid comparand to a first plurality of data lines that are electrically coupled to a first segment of CAM cells in the CAM array, while concurrently applying a data field of a second hybrid comparand to a second plurality of data lines that are electrically coupled to a second segment of CAM cells in the CAM array.

24. (Original) The method of Claim 23, wherein said applying step comprises applying the virtual sector field of the first hybrid comparand to the first plurality of data lines while concurrently globally masking a third plurality of data lines that are electrically coupled to a third segment of CAM cells in the CAM array.

25. (Original) The method of Claim 22, wherein said performing step comprises:

applying a virtual sector field and a first data field of a first hybrid comparand to a first plurality of data lines that are electrically coupled to a first segment of CAM cells in the CAM array, while concurrently applying a second data field of a second hybrid comparand to a second plurality of data lines that are electrically coupled to a second segment of CAM cells in the CAM array.

26. (Original) The method of Claim 25, wherein said applying step comprises applying the virtual sector field and the first data field of the first hybrid comparand to the

first plurality of data lines while concurrently globally masking a third plurality of data lines that are electrically coupled to a third segment of CAM cells in the CAM array.

27. (Original) A method of operating an integrated circuit system, comprising the steps of:

decoding a first portion of a first input address into sector, sub-sector and virtual sector addresses; and

performing a search operation in a sector of a CAM device that is designated by the sector address, by applying a first hybrid comparand comprising the virtual sector address and a second portion of the first input address, to first data lines that are electrically coupled to a CAM array within the sector.

28. (Original) The method of Claim 27, wherein said performing step comprises performing a pipelined search operation in the sector by applying the first search word while concurrently applying a portion of a second hybrid comparand to second data lines that are electrically coupled to the CAM array.

29. (Original) An integrated circuit system, comprising:

a multi-port memory array containing packet header data therein;

funnel logic that is configured to generate a N-bit comparand comprising portions of at least two header fields read from distinct locations in said multi-port memory array;

a content addressable memory device that is configured to generate an index in response to application of the N-bit comparand during a search operation; and

a memory device comprising an entry of microcode therein that is partitioned into at least a first field that identifies a write address in said multi-port memory array to which the index or data derived from using the index as a pointer is to be written.

30. (Original) The system of Claim 29, wherein said funnel logic comprises:

a multiplexer that is configured to receive read data from said multi-port memory array; and

a map table that is configured to pass select signals to said multiplexer, in response to a read address derived from a bit map field within the entry of microcode.

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